Recent developments of Silicon and Diamond Detectors Tracker Technologies for HL-LHC and beyond

Heinz Pernegger / CERN EP Department

With many thanks to colleagues who kindly provided material
Outline

• Silicon Tracker Upgrades towards the High-Luminosity LHC and beyond
• Developments for hybrid and monolithic pixel detectors in context of pp, ee and HI experiments
• Silicon tracker combined with timing capabilities
• Diamond Detectors for beam monitoring
High Luminosity - LHC

HL-LHC (High Luminosity LHC)
- Collisions to start after Long Shutdown 3 (2025-2027)
  - ~4000 fb⁻¹ Integrated luminosity to ATLAS/CMS over ten years
  - 200 (mean number of) interactions per bunch crossing.
    - Original design for 25 interactions per bunch crossing
  - Major upgrades of current silicon trackers for ATLAS & CMS in HL-LHC Phase 2 Upgrade projects
Challenges for the future

- Increased luminosity requires
  - Higher hit-rate capability
  - Higher segmentation
  - Higher radiation hardness
  - Lighter detectors

- Radiation hardness improvement compared to present trackers
  - factor 10 (HL-LHC) to factor 100 (FCC)
The environment at HL-LHC

- Radiation level, hit rates and bunch structure for silicon detector dominate the development of sensors and Front-end electronics
  - 25ns BC
  - L1 trigger rate (~1MHz)

- Strip layers
  - NIEL $\sim 10^{14} \, n_{eq}/cm^2$
  - TID $\sim 10$Mrad
  - Larger area $O(100m^2)$

- Outer pixel layers
  - NIEL $\sim 10^{15} \, n_{eq}/cm^2$
  - TID $\sim 50$Mrad
  - Larger area $O(10m^2)$

- Inner layers
  - NIEL $\sim 5\times10^{15}$ to $10^{16} \, n_{eq}/cm^2$
  - TID $\sim 1$Grad
  - Smaller area $O(1m^2)$
Beyond LHC: FCC/hh

- 4T, 10m solenoid, unshielded
- Forward solenoids, unshielded
- Silicon tracker
- Barrel ECAL LAr
- Barrel HCAL Fe/Scint
- Endcap ECAL/HCAL LAr
- Forward ECAL/HCAL LAr

50 m long, 20 m diameter

'general' purpose detector with very large $\eta$ acceptance and extreme granularity

Muon detection up to $\eta = 4$ ($\theta \approx 2^\circ$)  
Calorimetry up to $\eta = 6$ ($\theta \approx 0.5^\circ$)

L. Linssen/CERN
Granada 5/2019
Tracker at FCC/hh

Tracker radius 1.6 m, half-length 16 m, initial baseline hit position resolution 7–9 μm in Rφ

- High occupancies => small cell sizes (~25×50 μm² in inner layers)
- Two-track separation in boosted objects
  - small cell sizes + better hit resolution <5 μm
- Tilted layout to minimize multiple scattering
- High-E => significant fraction of displaced vertices outside acceptance
- Radiation ×100 higher than present technologies

L. Linssen/CERN
Granada 5/2019
High-energy $e^+e^-$ colliders

**CLIC** => CLICdet, vs: 380 GeV, 1.5 TeV, 3 TeV

**FCC-ee** => CLD and IDEA, vs: 90 - 365 GeV

**ILC** => ILD and SiD: vs: 250 – 500 GeV (1 TeV)

**CEPC** => baseline and low-B vs: 90-240 GeV
Hybrid pixel sensors

- Front-end chip
  - Depending on application we need specialized FE-ASIC
  - Complexity of designs are driven by experimental needs
  - Increasing functionality on chip drives the development towards 65nm and smaller node size CMOS processes

- Sensor developments
  - For very high radiation and track density (e.g. 3D sensors, active edge planar)
  - Sensors for 4D tracking, i.e. spatial and time information (e.g. pixel sensors with trench electrodes)
Future Trackers at ATLAS and CMS

Sensor active thickness 100 - 300 µm

**ATLAS Simulation Preliminary**

- Inclined Duals
- η = 1.0
- η = 2.0
- η = 3.0

**3D sensors**

- Stereo
- Planar Sensors - Strips
- Planar Sensor Pixel

**Trigger inside**

- No Stereo inside

- η < 4

**Planar Sensors**

- Planar Macro-pixel
- Planar Micro-pixel

**All n-in-p sensors inside with different thicknesses**
Next generation Pixel Detectors

Many commonalities ATLAS – CMS lead to RD53 Developments

- “Classical” hybrid pixel detectors with bump-bonding
  - THIN Planar n-on-p or 3D detectors (inner layers)
  - Common R&D on chip RD53A– 65nm TSMC
  - Modules: Single to Quads chip arrangements
- Common design of pixel FE-IC implemented with different matrix size and FE design
  - Sensor 50 x 50 µm pitch
  - Sensor 25x100 µm pitch
- Serial Powering (part of RD53)
- Both detectors up to $\eta=4$

Surface: 2*CMS < 1*ATLAS
First RD53B tests

- One bug in ToT memory to fix, otherwise good performance
- Good data transmission and PLL results, noise and threshold behavior
- Direct access to analog information through precision ToT
- First tests on serial powering ShuntLDO
- First SEU tests done
Sensors for hybrid detectors

ATLAS/CMS

• 3D and Planar sensors developed to radiation hardness of \(10^{16} \text{n}_{\text{eq}}/\text{cm}^2\) for HL-LHC on 4”, 6”, 8” wafer
  • Further development focuses on
  • Better lithography for smaller pixels on 3D
  • Optimizing active edge on planar
  • Move to 8” wafers

• Special sensor for timing application in pixel sensor
PixelVelo and Upstream Tracker for LHCb in LS2

Maintain Physics Performance in very high occupancy and pile up conditions.
Combinatorial complexity and fake tracks.
Pile-up energy mitigated by granularity, high readout speed and trigger innovations.
Timing will be for Upgrade II.

Operate with detector elements exposed to very high radiation doses.
Radiation hardness needed for all subdetectors.

Cope with tremendous DAQ and data processing challenges.

PixelVelo Stations assembled
VeloPix for LHCb Upgrade 1

Derived from Timepix3 and dedicated to LHCb.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel arrangement</td>
<td>256 x 256</td>
<td></td>
</tr>
<tr>
<td>Pixel size</td>
<td>55 x 55 µm²</td>
<td></td>
</tr>
<tr>
<td>Peak hit rate</td>
<td>80 Mhits/s/ASIC</td>
<td>800 Mhits/s/ASIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50 khits/s/pixel</td>
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<tr>
<td>Readout type</td>
<td>Continuous, trigger-less, TOT</td>
<td>Continuous, trigger-less, binary</td>
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<tr>
<td>Timing resolution/range</td>
<td>1.5625 ns, 18 bits</td>
<td>25 ns, 9 bits</td>
</tr>
<tr>
<td>Total Power consumption</td>
<td>&lt;1.5 W</td>
<td>&lt; 3 W</td>
</tr>
<tr>
<td>Radiation hardness</td>
<td></td>
<td>400 Mrad, SEU tolerant</td>
</tr>
<tr>
<td>Sensor type</td>
<td>Various, e- and h+ collection</td>
<td>Planar silicon, e-collection</td>
</tr>
<tr>
<td>Max. data rate</td>
<td>5.12 Gbps</td>
<td>20.48 Gbps</td>
</tr>
<tr>
<td>Technology</td>
<td>IBM 130 nm CMOS</td>
<td>TSMC 130 nm CMOS</td>
</tr>
</tbody>
</table>
Timing for tracking

Need sub-nanosecond track time to suppress background in environments with large pile-up (HL-LHC, FCC) → 4D tracking

Separate timing layers with coarser granularity → timing for reconstructed tracks (e.g. HL-LHC upgrades ~30 ps)

Timing within pixel layers → time info for pat rec (e.g. LHCb Upgrade II 20-200 ps, depending on pixel size, radiation)

→ Trade-off between time resolution and pixel size / layer thickness
→ FCChhh needs track timing at 5 ps up to $6 \times 10^{17}$ $n_{eq} / \text{cm}^2$ fluences
Timing sensors for tracking

LHCb: timing will be needed in future upgrades to associate secondary vertices correctly to primary vertices.

LHCb studies show that with just 200 ps per hit, misassociation rate drops to Phase I levels of < 1%

V. Gligorov

P. Collins / CERN LHCb

H. Pernegger/CERN Dec 15, 2020
Timing Sensors for Tracking

- Very promising advances for 3d detectors e.g. from TIMESPOT collaboration & R&D with FBK:

Adriano Lai/Cagliari – Vertex 2020

Electronics

Sensor
LGAD timing sensors

Low Gain Avalanche Detectors (LGAD): Multiplication of charges (~10-100x) in thin gain layer \( \rightarrow \) fast rise time, increased S/N

- Several vendors: CNM, FBK, HPK
- Reached \(~30\) \( \text{ps} \) for few \( \text{mm}^2 \) size sensors \( \rightarrow \) used for HL-ATLAS & CMS timing layers

Limiting factors for time resolution:
- Weighting field uniformity \( \rightarrow \) favors larger pixels
- Radiation effects \( \rightarrow \) ok up to \(~10^{15}\), mitigation measures under study for higher fluences
- \( r/o \) electronics + clock distribution \( \rightarrow \) IC work package

- R&D to achieve radiation hardness
  - Variation in doping to limit gain loss after irradiation
- RD for larger fill factors (currently \(~70-00\) \( \mu \text{m} \) inactive region between pixels):

F. Carnesecchi / Frontier Detectors – Elba 2018
**LGAD: Gain layer engineering**

**Defect Engineering of the gain layer**
- Carbon co-implantation mitigates the gain loss after irradiation
- Replacing Boron by Gallium did not improve the radiation hardness

**Modification of the gain layer profile**
- Narrower **Boron doping profiles** with high concentration peak (Low Thermal Diffusion) are less prone to be inactivated
- Deep Gain Layer improves electric field after acceptor removal (see N. Cartiglia, Hiroshima 2019 HST12)

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**Graph**

- **Boron + Carbon**
- **Gallium + Carbon**
- **Boron (Low Diff)**
- **Boron (High Diff)**
- **Gallium**

**RD50 Status Report 2019 - M.Moll - G.Casse and Vertex 2020 workshop**
CMS and ATLAS timing layers

- Dedicated FE-chips bump-bonded to LGAD sensors
Monolithic Silicon Pixel Detectors

Depleted Monolithic Active Pixel Sensors

- Depletion is key for fast signal response and radiation hardness
- Thin detector with high granularity

- FE electronics is integrated in sensor and produced on commercial CMOS processes
- Allows very thin sensors to achieve ultimate low mass trackers (0.3% $X/X_0$)
- High volume and large wafers (200mm) reduces detector costs and allows large area pixel detectors
- Saves costs of bump-bonding (cost driver for hybrid silicon detector systems)
**DMAPS/CMOS for Future Trackers**

<table>
<thead>
<tr>
<th></th>
<th>RHIC STAR</th>
<th>LHC - ALICE ITS</th>
<th>CLIC</th>
<th>HL-LHC Outer Pixel</th>
<th>HL-LHC Inner Pixel</th>
<th>FCC pp</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NIEL ([n_{eq}/cm^2])</strong></td>
<td>(10^{12})</td>
<td>(10^{13})</td>
<td>&lt;(10^{12})</td>
<td>(10^{15})</td>
<td>(10^{16})</td>
<td>(10^{15-10^{17}})</td>
</tr>
<tr>
<td><strong>TID</strong></td>
<td>0.2Mrad</td>
<td>&lt;3Mrad</td>
<td>&lt;1Mrad</td>
<td>80 Mrad</td>
<td>2x500Mrad</td>
<td>&gt;1Grad</td>
</tr>
<tr>
<td><strong>Hit rate [MHz/cm²]</strong></td>
<td>0.4</td>
<td>10</td>
<td>&lt;0.3</td>
<td>100-200</td>
<td>2000</td>
<td>200-20000</td>
</tr>
</tbody>
</table>

- **Advances in commercial CMOS technologies combined with dedicated designs allowed significant progress from STAR to ALICE to ATLAS in areas like radiation hardness, response time, hit rates.**
- **Strong interest for R&D to fully exploit potential of MAPS in future Trackers**
  - High granularity, Low material budget and power, Large area at reduced cost (cf hybrid)
  - CMOS foundries offer substantial processing power to enable significant performance gains

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**Ultimate Sensor**

**Alpide Sensor**

**Monopix & AtlasPix & Malta Sensor**

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DAE-BRNS HEP Symposium 2020
ALICE Inner Tracking System Upgrade at LHC

Based on high resistivity epi layer MAPS

3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

Radial coverage: 21-400 mm

~ 10 m²

|η|<1.22 over 90% of the luminous region

0.3% $X_0$/layer (IB)
0.8 % $X_0$/layer (OB)

Radiation level (L0): 700 krad/$10^{13} \text{ n}_{\text{eq}} \text{ cm}^{-2}$

Installation during LS2 (2019-2020)
ALICE ITS Layer Assembly

Layers assembly L5 Top on L6 Top

C. Gargiulo, CERN

ITS2 assembled and commissioned on surface
ALICE ITS3 Proposal for LS3


L. Musa, CERN
https://indico.cern.ch/event/755366/

Vertex Detector (innermost 3 layers)

EoI for new ultra-light Inner Barrel in LS3 (CDS, ALICE-PUBLIC-2018-013)

Recent silicon technologies (ultra-thin wafer-scale sensors) allow

- Eliminate active cooling ⇔ possible for power < 20mW/cm²
- Eliminate electrical substrate ⇔ Possible if sensor covers the full stave length
- Sensors arranged with a perfectly cylindrical shape ⇔ sensors thinned to ~30μm can be curved to a radius of 10-20mm

Truly cylindrical vertex detector

Beampipe
IR: 16 mm
ΔR: 0.5 mm

Pipe: r ≈ 16 mm, ΔR = 0.5 mm
L0: r = 18 mm, L1: r = 24 mm, L2: r = 30 mm

0.05% x/X₀ per layer

Open cell carbon foam
Towards wafer-scale integration

- Starting from ALPIDE architecture by porting to 65 nm technology node
  - smaller pixels
  - larger wafers (300 mm instead of 200 mm)
- Basic building block of 15 mm height
  - to be repeated n times in vertical direction to obtain the sizes needed per layer
Detector developments for CLIC

CLIC tracking system - requirements & challenges

Compact Linear Collider CLIC

Linear $e^+e^-$ collider proposed for post-LHC phase at CERN
- $\sqrt{s}$ up to 3TeV (staged scenario), small beam size (40nm x 1nm x 44μm)
→ Challenging environment: high rates from beam-induced background

Requirements for vertex & tracker:

Low mass:
- 0.2 % $X_0$ / layer in vertex detector
→ Forced air flow cooling

→ Low power:
- 50mV/cm$^2$ in vertex detector
→ Power pulsing of electronics

Precise spatial resolution
- 3μm in vertex and 7μm in tracker
→ Fine pitch (25μm in vertex)
Precise timing resolution: ~5ns
→ Mitigate impact of hits from beam-induced background
Detector developments for CLIC

Monolithic silicon pixel detectors for CLIC

Why monolithic?:
Large area production with low costs, reduced material

Challenges:
Impact of circuitry on sensor and vice versa

CLICTD – a fully integrated small collection electrode HR-CMOS chip for the CLIC tracker:

180nm modified CMOS imaging process
30µm x 37.5µm pixel size
Implemented on epitaxial layer of 30µm
8 pixels combined in common digital channel:

Results, modified process, bias p-well/substrate -3V/-6V:
- Noise \( \sim 15e^- \), minimum threshold \( \sim 245e^- \) (ongoing work)

- Efficiency \( \sim 99\% \)
- Timing resolution 10ns after time-walk correction (ongoing work)
- Next: testing of thinned samples (down to 40µm)

→ Reduce digital circuitry while maintaining speed of charge collection
- 8-bit ToA and 5-bit ToT measurement per channel, storage of hit-pattern on pixel level
- Gap in n-layer along beam-dimension to speed up charge collection & reduce charge shared within channel
Detector developments for CLIC

Simulations of small collection electrode CMOS

Optimization of small collection electrode CMOS sensors - 3D TCAD:

- Higher capacitance due to non depleted regions around collection electrode for:
  - Larger opening of p-wells
  - Lower p-well voltage
  - Higher n-layer dose

→ Optimization in 3D TCAD necessary

Electric field & depletion around collection electrode for different openings:

Capacitance for different openings:

Simulation of full detector response with 3D TCAD and Allpix2 Monte Carlo framework:

- Gap in n-layer:
  - Bending field lines towards collection electrode → less charge sharing

- In-homogenous field over pixel cell
  → Modelling of full response in Allpix2 necessary

In-pixel cluster size no gap in n-layer:

In-pixel cluster size, gap in n-layer along x:

CLICdet work in progress

D. Dannheim / M. Munker

H. Pernegger/CERN Dec 15, 2020

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Towards radiation hard MAPS...

...there were several obstacles to overcome:

Depletion is key:

- At high radiation levels (>10^{16} \text{n}_{\text{eq}/\text{cm}^2}) the ionization charge is trapped in the non-depleted part
- Diffusion makes signal collection slower than typical requirements for pp-colliders

Readout architectures are low power but not designed for high hit-rates of pp experiments at LHC or future pp colliders
Different CMOS sensor designs

- Purse different design approaches for optimal performance

- **Large electrodes**
  - Electronics in collection well
  - No or little low field regions
  - Short drift path for high radiation hardness
  - Large(r) sensor capacitance \( \frac{dpw}{dnw} \) -> higher noise and slower @ given pwr
  - Potential cross talk between digital and analog section

- **Small electrodes**
  - Electronics outside collection well
  - Small capacitance for high SNR and fast signals
  - Separate analog and digital electronics
  - Large drift path -> need process modification to usual CMOS processes for radiation hardness

- **“Burried” electrodes (SOI)**
  - Electronics and sensor in separate layer
  - Can use thick or thin high resistivity material and HV (>200V)
  - Special design/processing to overcome radiation induced charge up of oxides
Radiation hard CMOS sensor

\[ d \sim \sqrt{\rho \cdot V} \]

1. “High” Voltage add-ons to apply 50 – 200 V bias

I. Peric, NIM A582 (2007) 876-885

2. “High” Resistivity Substrate Wafers (100 Ωcm – kΩ cm)

3. Multiple (3-4) nested wells (for shielding and full CMOS)

from: www.xfab.com

4. Backside Processing (for thinning and back bias contact)

Effective resistivity after HL-LHC irradiation \( \sim O(100\,\Omega\text{cm}) \)
ATLAS CMOS Sensors Development Lines

- Developed in context of ATLAS CMOS collaboration by ~25 institutes together with the EU project “STREAM” – apply all knowledge to large size monolithic sensor
- Special focus different high-performance readout architectures to cope with high hit rates, high frame rate/speed and high radiation
HVCMOS sensors (AMS 180nm)

Developments in context of ATLAS and μ3e experiment using large n-electrodes in different HR substrates

**ATLASPix1 M2**
- 320×56 pixel matrix
- 50×60 µm² pixel size
- triggered readout

**ATLASPix1 Simple**
- 400×25 pixel matrix
- 40×130 µm² pixel size
- asynchronous Readout of signal to periphery with “column drain”-type buffer/ToT in periphery

>99% after $10^{15} \text{n}_{eq}/\text{cm}^2$
LFoundry ATLAS prototypes

- Developed sensors in 150nm process on 2kΩcm substrates
Hit efficiency of LF-Monopix

- **Un-irradiated**
  - DAC setting: default
  - TH: tuned by noise + 4mV (~1750e)
  - HV: -200V
  - Temp: dry ice
  - Source: ELSA 2.5GeV electron

- **$1 \times 10^{15} n_{eq}/cm^2$**
  - DAC setting: default
  - TH: tuned by noise (~1500e)
  - HV: -130V
  - Temp: dry ice
  - Source: ELSA 2.5GeV electron

99.6% 98.9%

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T. Hirono et al 2019 NIMA 924 87

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Novel CMOS Pixel with small electrodes

- Small collection electrode (few um²)
- **Small input capacitance (<3fF) allows for fast & low-power FE**
- High S/N for a depletion depth of ~20um
- To ensure full lateral depletion, uniform n-implant in the epi layer (modified process)

![Diagram showing standard and modified processes](image)

**Standard Process**

**Modified Process**


H. Pernegger et al 2017 JINST 12 P06008
TJ MALTA & TJ MonoPix – Novel depleted CMOS sensors with small electrodes

- The ATLAS “MALTA” and “MonoPix” chips for high hit rate suitable for HL-LHC pp-collisions
  - Radiation hard to $>10^{15}$ n/cm² & Shaping time 25ns (BC = 25ns)
  - **MALTA**: Asynchronous readout architecture for high hit rates and fast signal response
  - **MonoPix**: Synchronous Column drain readout architecture
New TJ-MALTA on HR Cz substrate

• Original MALTA design reprocessed on high resistivity Cz substrate material with new implant geometries for best signal collection
• Allows for significant larger depletion and signal
• Even higher radiation hardness and possible improved time-resolution with O(ns)
• Input for future Version 2 sensor matrixes in MALTA and MonoPix design
• Requires careful engineering to avoid punch-through and high operation voltages
Efficiency MALTA-Cz

- n-irradiated (IJS) followed by DESY beam test
- Preliminary Efficiency (shown as 2x2 pixel x-y dependency) compared unirradiated – 1x10^{15} n_{eq}/cm^2 - 2x10^{15} n_{eq}/cm^2

MALTA Cz unirradiated

\[ \varepsilon = 98.8\% \]

Sector 2, \(<\text{eff}> = 98.5\pm0.0\% \)

MALTA Cz n-gap 1x10^{15} n_{eq}/cm^2

\[ \varepsilon = 97.1\% \]

Sector 2, \(<\text{eff}> = 97.0\pm0.0\% \)

MALTA Cz n-gap 2x10^{15} n_{eq}/cm^2

\[ \varepsilon = 95.4\% \]

Sector 2, \(<\text{eff}> = 95.4\pm0.0\% \)

Thres = 427 e^{-} 
ENC = 9.8 e^{-}

Thres = 260 e^{-} 
ENC = 12.7 e^{-}

Thres = 226 e^{-} 
ENC = 14 e^{-}
Time resolution & Cluster size
MALTA Cz

- Substantially more charge sharing in Cz material than in epitaxial substrates
- Cluster size depends on substrate voltage and implant geometry as depletion depth & drift path changes in Cz substrate
- Time resolution <2ns
CVD Diamond Detectors

- Developed as radiation hard detectors with large band gap for LHC largely in context of beam monitoring for ATLAS, CMS and ALICE
  - Beam conditions or beam loss monitor
  - pCVD and scCVD diamonds typically 5x5 to 10x10mm$^2$
- For HL-LHC and similar applications a new generation of CVD diamond detector systems are being developed
  - Fast bunch-by-bunch safety system
  - Luminosity measurement
  - Background monitors

Charge collection distance
\sim 400 \mu m on pCVD

M. Mikuz, IJS, Slovenia

ATLAS BCM'

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3D diamond detectors

- Femtosecond laser converts insulating diamond to resistive mix of carbon phases
- This allows to create electrodes inside the diamond bulk similar to 3D silicon sensors
  - Cell size currently 50x50 µm²
  - Electrode 2.6 µm diameter
  - Column yield 99%

Bump-bonded to CMS pixel chip

HV=-55V;
Efficiency >99.2%

H. Kagan/ OSU presentation ICHEP2020
Radiation hardness of CVD diamond

- RD42 determines diamond radiation damage constant for different species/energies measured through \( \frac{1}{\text{mean free path}} = \frac{1}{\lambda} \)

- Test rate dependence of diamond signal before and after irradiation

<table>
<thead>
<tr>
<th>Irradiation Species</th>
<th>( k_i )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast neutrons</td>
<td>( 4.31 \pm 0.34 )</td>
</tr>
<tr>
<td>70 MeV protons</td>
<td>( 2.65 \pm 0.25 )</td>
</tr>
<tr>
<td>800 MeV protons</td>
<td>( 1.67 \pm 0.09 )</td>
</tr>
<tr>
<td>24 GeV protons</td>
<td>1</td>
</tr>
</tbody>
</table>
Looking towards the future

There are very challenging targets ahead at HL-LHC and future collider experiments for new silicon detectors.

- **Radiation hard, thin and small pixel Vertex layers** for very high hit-rates at innermost layers.
- **Merge tracking and timing**: how about a 10x10\(\mu\)m\(^2\) pixel with 10ps timing? A dream for reconstruction.
- **Ultra-thin detectors**: reduced multiple scattering to maybe 1/10\(^{th}\) of today?

4D tracking
Summary

- The required functionality from silicon tracking detectors leads to more and more complex detector systems to cope with accelerator’s present and future performance.

- The need for these new complex systems has triggered a large RD effort in the area of sensors, electronics and detector integration.

- Hybrid pixel detector for HL-LHC cope with enormous radiation level and hit rates together with sophisticated on-chip data handling.

- Monolithic CMOS sensors are being developed for high-radiation environments with complex readout architectures for future large pixel systems.

- The combination of timing and tracking leads to the development of new sensors for new level of performance in future silicon system with LGAD sensors.

- Developing and integrating these sensors to modules and systems leads to many new RD collaborations with semiconductor industry for manufacturing and post-processing.